

AMENDMENTS TO THE CLAIMS

1. (Original) In an integrated circuit multichannel packet transfer device, a multichannel interval timer for generating a time-out pulse for each of a plurality of transfer channels, comprising:

a counter comprising a first plurality of bits configured to increment through a multi-bit count in a free running loop;

for each of the plurality of transfer channels, a selection circuit for selecting from a plurality of input signals to generate a selected output signal in response to a control signal, where each of the plurality of input signals is coupled to a respective one of the first plurality of bits of the counter;

a control signal generator coupled to each selection circuit for generating a control signal for each transfer channel; and

a pulse generator coupled to the selected output signal from each selection circuit to generate a time-out pulse for each transfer channel whenever a transition in the selected output signal is detected, wherein the time-out pulse timing for each transfer channel is determined by the control signal.

2. (Original) The interval timer recited in claim 1, wherein each control signal generator comprises a timer control register for storing a time-out setting.

3. (Original) The interval timer recited in claim 1 formed in a packet manager input circuit wherein the plurality of transfer channels comprises a first input channel and a second input channel.

4. (Original) The interval timer recited in claim 1, where the plurality of transfer channels comprises a plurality of virtual channels.

5. (Original) The interval timer recited in claim 1, further comprising a control circuit for transferring data received on a first transfer channel to memory by releasing one or more descriptors associated with said first transfer channel, where said

control circuit is coupled to receive the time-out pulse for each transfer channel and is configured to delay release of said one or more descriptors until after receiving the time-out pulse for said first transfer channel.

6. (Original) The interval timer recited in claim 5, wherein a plurality of descriptors received before the time-output pulse is generated are released together with a write-invalidate command.

7. (Original) The interval timer recited in claim 5, wherein a plurality of descriptors are released sequentially with read-modify-write commands when only one of the plurality of descriptors is received before the time-output pulse is generated.

8. (Original) The interval timer recited in claim 1, wherein each selection circuit comprises a multiplexer for each transfer channel, where each multiplexer has a plurality of inputs corresponding to the plurality of bits in the counter, such that each multiplexer passes one of the plurality of bits of the counter to the pulse generator.

9. (Original) The interval timer recited in claim 1, further comprising an interrupt control circuit for issuing an interrupt signal once a threshold number of packets are transferred, where said interrupt control circuit is coupled to receive the time-out pulse for each transfer channel and is configured to force issuance of an interrupt signal upon receiving the time-out pulse, even if the fewer than the threshold number of packets are transferred before the time-out pulse is received.

10. (Original) An apparatus comprising:
a first interface circuit for receiving and transmitting packet data on a first channel;
a second interface circuit for receiving and transmitting packet data on a second channel;
a memory;

a packet manager circuit coupled to receive data on the first channel from the first interface circuit and to receive data on the second channel from the second interface circuit, wherein the packet manager circuit is configured to transmit data on the first and second channels to the memory under control of at least a first descriptor and a second descriptor, respectively, said packet manager being further configured to write back said at least a first descriptor to memory under control of a first time-out signal and to write back said at least a second descriptor to memory under control of a second time-out signal; and

a timer for generating the first and second time-out signals, comprising

a multi-bit counter,

a first and second multiplexer, each multiplexer having a select line, an output and multiple inputs, with each input coupled to a corresponding bit of the multi-bit counter,

a first and second timer control register coupled respectively to the select lines of the first and second multiplexers, and

a first and second pulse generator coupled to each multiplexer output for generating first and second time-out signals,

wherein the first multiplexer selects one of the bits in the multi-bit counter for output to the first pulse generator in response to the first timer control register to generate the first time-out signal, and the second multiplexer selects one of the bits in the multi-bit counter for output to the second pulse generator in response to the second timer control register to generate the second time-out signal.

11. (Original) The apparatus recited in claim 10, wherein the first interface circuit, second interface circuit, packet manager circuit and timer are constructed on a single integrated circuit substrate.

12. (Original) The apparatus recited in claim 10, wherein the first timer control register stores a timer interval value for the first channel.

13. (Original) The apparatus recited in claim 12, wherein the timer interval value for the first channel may be programmably selected from a plurality of

timer interval values by selecting a bit from the multi-bit counter, where a selected timer interval value measures a transition in the selected bit of the multi-bit counter.

14. (Original) The apparatus recited in claim 10, wherein the multi-bit counter comprises a plurality of bits coupled in sequence and configured to run in a free running loop.

15. (Original) The apparatus recited in claim 10, wherein the packet manager circuit transfers a plurality of descriptors together on the first channel if the plurality of descriptors are received before the first time-out signal is generated, but transfers the plurality of descriptors in sequence on the first channel if only one of the plurality of descriptors is received before the first time-out signal is generated.

16. (Original) The apparatus recited in claim 10, further comprising an interrupt controller for controlling the issuance of interrupts from the packet manager, such that the interrupt controller issues interrupts after a specified number of packets are processed, unless the second time-out signal is generated, in which case any available interrupts for the second channel are issued.

17. (Original) A method for generating time-out signals for a plurality of channels, comprising:

running a free-running timer in a loop;
generating a first pulse whenever a transition is observed in a first selected bit position of the free-running timer, where said first pulse comprises a first time-out signal.

18. (Currently Amended) The method recited in claim 17, where[[in said]] running [[a]] the free-running timer comprises incrementing a multi-bit counter through a free-running loop.

19. (Currently Amended) The method recited in claim 18, where[[in said]] generating [[a]] the first pulse comprises selectively coupling a first bit of the multi-bit

counter to a first pulse generator in response to a first timer interval control signal and generating [[a]] the first pulse as a first time-out signal.

20. (Original) The method of claim 19, wherein said selectively coupling comprises issuing the first timer interval control signal as a select signal to a multiplexer with each of its inputs coupled to each bit in the multi-bit counter, to thereby select one of the inputs for output by the multiplexer to the first pulse generator.